IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney 13361US02

In the Application of: Buer		)
U.S. Serial No.:	10/757,259	)
Filed:	1/14/2004	)
Examiner:	Hur	)
Group Art Unit:	2824	)

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This is an appeal from the Office Action made Final mailed 11/24/09. A Notice of Appeal was duly filed with the United States Patent and Trademark Office on 4/9/10.

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I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine California 92618-3616, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefore, as set forth in the Assignment filed with the present application and recorded on February 20, 2002 at Reel/Frame 012614/0038.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,996,091 ("Jones") in view of U.S. Patent 6,611,040 ("Gelsomini").

Claims 2-3 are cancelled.

Claims 4-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of Gelsomini.

Claims 11-12 are cancelled.

Claims 13-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of Gelsomini.

Claims 15 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of Gelsomini and further in view of U.S. Patent 5,996,091 ("Giolma").

Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of Gelsomini.

Claims 18-19 are cancelled.

Claim 20 and 21 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of Gelsomini and further in view of Giolma.

Claim 22 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of Gelsomini.

Claims 1, 4-10, 13-17, 20-22 are appealed.

IV. STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a method of verifying a state of an element comprising:

determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element (Specification at 5, Lines 9-10); and

outputting a valid signal if the state of the element is equal to said expected state, wherein the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick (Specification at 5, Lines 10-11).

Claim 9 is a method for verifying a state of a memory device comprising:

comparing a state of a first thin oxide gated fuse having an oxide that is less than 2.5 nm thick (Specification at 15, Lines 5-12), to a first expected state and generating a first signal, wherein the state is a state of electrical resistance (Specification at 16, Lines 1-5);

comparing a state of a second thin oxide gated fuse having an oxide that is less than 2.5nm thick (Specification at 15, Lines 5-12), to a second expected state, and generating a second signal, wherein the state is a state of electrical resistance (Specification at 16, lines 6-13); and

outputting a valid signal if both said first and second signals are the same (Specification at 16, lines 17-18).

Claim 17 is directed to a method for verifying a state of a thin oxide gated fuse memory device, comprising:

setting a first expected state (Specification at 9, line 2);

sensing a state of a first thin oxide gated fuse having an oxide that is less than 2.5nm thick, wherein the state is a state of electrical resistance (Specification at 16, Lines 1-5);

determining if said state of said first thin oxide gated fuse is equal to said first expected state and generating a first signal (Specification at 16, Lines 1-5);

setting a second expected state (Specification at 9, line 2);

sensing a state of a second thin oxide gated fuse having an oxide that is less than 2.5nm thick, wherein the state is a state of electrical resistance (Specification at 16, lines 6-13);

determining if said state of said second thin oxide gated fuse is equal to said second expected state and generating a second signal (Specification at 16, lines 6-13); and

generating a valid output if both said first and second signals are the same (Specification at 16, lines 17-18).

Claim 20 is directed to a memory device comprising:

at least one memory cell (Figure 2, OTP Cell 112) having at least one thin oxide gated fuse (Specification at 10, Line 13, Figure, 2, Fuse 122, 124) having an oxide that is less than 2.5nm thick (Specification at 15, Lines 5-12);

at least one reference cell (Specification at 9, Line 26, Figure 1, Reference Cell 14);

at least one verify circuit connected to said memory cell and said reference cell sensing a state of said at least one thin oxide gated fuse, wherein the state is a state of electrical resistance (Specification at 10, Line 21, Figure 2, Verify Circuit 116);

at least one exclusive nor gate connected to said verify circuit (Specification at 11, Lines 5-6, Figure 2, 118); and

a logic gate connected to said exclusive nor gate generating a valid signal (Specification at 11, line 8; Figure 2, 132).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims Claims 1, 4-10, 13, 14, 17, and 22 are obvious from Jones and Gelsomini.

Whether claims 15, 16, 20, and 21 are obvious from Jones, Gelsomini, and Giolma.

VII. ARGUMENT: CLAIM 1

Claim 1 is copied below:

> A method of verifying a state of an element comprising:
>
> determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element; and
>
> outputting a valid signal if the state of the element is equal to said expected state, wherein the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick.

Claim 1 was rejected under 35 U.S.C. 103(a) as being obvious from Jones in view of Gelsomini. Appellant respectfully submits that the rejection to claim 1 should be reversed because (1) of unexpected results at the range of <2.5nm; and (2) Jones and Gelsomini do note teach the claimed "determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element".

A. THE REJECTION TO CLAIM SHOULD BE REVERSED BECAUSE THE CLAIMED < 2.5NM PROVIDES UNEXPECTED RESULTS.

Claim 1 recites, among other limitations, "wherein the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick". The Office Action has indicated that "JONES does not disclose that the element comprises a thin gated fuse having a oxide that is less than 2.5 nm thick and the state of the element is a state of the electrical resistance of the element. GELSOMINI discloses a thin oxide gate fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6 and claim 5)...". Office Action at 4.

Gelsomini teaches "Gate oxide anti-fuses have gate insulators made of silicon dioxide in a thickness range from about 2 to 10nm." Col. 4, Lines 3-4. The Office Action also cites MPEP 2144.05.I. Although the claimed range < 2.5nm and the range disclosed in Gelsomini, 2-10nm overlap, "Applicants can rebut a *prima facie* case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)." MPEP 2144.05.III.

Assignee respectfully submits that the claimed range, < 2.5nm achieves unexpected results relative to the prior art range. Paragraph 0011 of 09/739,752,

which is incorporated by reference in the present application, 0009, "The oxide is about 20 Angstroms thick, which allows direct tunneling current and yields an after-programmed resistance on the order of a few hundred ohms or less, *which is an order of magnitude lower then conventional one-time programmable anti-fuses*. Voltage to rupture gate oxide can be adjusted depending on the programming time pulse and final resistance spread requirement." Additionally, paragraph 0029 of 09/739,752 states that the claimed range has properties not possessed by the prior art, "The gate oxide layer is approximately 20 Angstroms thick, which can be achieved with 0.13 um or less process technology. This thickness is chosen so that the gate can be ruptured by direct tunneling gate current, rather than Fowler-Nordheim tunneling." "Presence of a property not possessed by the prior art is evidence of nonobviousness. *In re Papesch*, 315 F.2d 381, 137 USPQ 43 (CCPA 1963). MPEP 716.02(a).

In response, Examiner has indicated that:

> "when one of ordindary skill in the art selects a thickness < 2.5nm as an optimum value in view of the Gelsomini's teaching of an oxide thickness range 'from about 2 to 10nm', one would expect a direct tunneling current and an after-programmed resistance of an order of magnitude lower than that of conventional programmable anti-fuses (presumably with a thick oxide), as a result of the oxide thickness."

Appellant respectfully submits that the rejection is in error. It is noted that an order of magnitude is a significant drop-off in resistance. Compare an order of magnitude to the ratio 10nm, the top of Gelsomini's range, to 2.5nm, only four-fold.

Furthermore, no evidence is provided to establish the fact that "one would expect a direct tunneling current and an after-programmed resistance of an order of magnitude lower than that of conventional programmable anti-fuses (presumably with a thick oxide), as a result of the oxide thickness."

B. THE REJECTION SHOULD BE REVERSED BECAUSE THE COMBINATION OF JONES AND GELSOMINI DOES NOT TEACH "DETERMINING IF THE STATE OF THE ELEMENT IS EQUAL TO AN EXPECTED STATE USING A VERIFY CIRCUIT, WHEREIN THE STATE OF THE ELEMENT IS A STATE OF THE ELECTRICAL RESISTANCE OF THE ELEMENT".

Additionally, claim 1 recites, among other limitations, "determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element". The Office Action indicates that Jones discloses "determining if the state of the element is equal to an expected state (VERIFY DATA 0 in Fig. 3b) using a verify circuit (308 in Fig. 3a); and outputting a valid signal (FAST VERIFY OUTPUT of 390 in Fig. 3b) if the state of the element is equal to said expected state (if DR0 is equal to VERIFY DATA 0 in Fig. 3b;". Examiner has also indicated that Gelsomini teaches "a thin oxide gated fuse … wherein a state of the fuse is a state of the electrical resistance of the fuse (inherent as a fuse)." Examiner also indicated that "It would be obvious at the time the invention was made … to substitute a thin oxide gated fuse … as an equivalent memory element … such that the state of the element is a state of the electrical resistance of the element".

Appellant respectfully submits that the rejection is in error because Jones and Gelsomini do not teach "determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element". Structure 308, which Examiner has indicated that the "verify circuit" which is used for "determining if the state of the element (DR0 in Fig. 3b) is equal to an expected state (VERIFY DATA 0 in Fig. 3b) are (further illustrated in Figure 3b) XOR gates. While XOR gates measure signals – the XOR gates do not measure electrical resistance.

Examiner has responded that "when Gelsomini's fuse/antifuse is substituted for the memory element in the Jones/Gelsomini combination, in obtaining the VERIFY DATA 0 signal in Fig. 3b of Jones, although it may be a

logic signal, it is inherently determined by, or based on a state of the electrical resistance/conductivity of the fuse/antifuse.

Appellant submits that the foregoing is in error. As an initial matter, Examiner provides no reasoning as to why VERIFY DATA 0 signal is inherently based on a state of the electrical resistance/conductivity of the fuse/antifuse. Secondly, it is not inherent. VERIFY DATA 0 is the output of an XOR gate. The output of an XOR gate is entirely determined by the signal levels of the inputs. Moreover, the output of the XOR gate would not reveal the state of the electrical resistance of the fuse/antifuse. For example, if the fuse/antifuse is in a state of zero electrical resistance, the output of the XOR gate can still be either 0 or 1. Accordingly, the an XOR gate, element 308 is inoperable to determine "if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element".

Accordingly, for at least the foregoing reasons, the rejection to claim 1 should be REVERSED.

VIII. ARGUMENT: CLAIM 9, 17, AND 20

Appellant incorporate Section VII.A herein, and submits that claims 9, 17, and 20 should also be REVERSED for the reasons therein.

CONCLUSION

For the foregoing reasons, claims 1-8 and 15-22 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

Dated: October 12, 2010

Mirut P. Dalal
Registration No. 44,052
Attorney for Appellant

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, IL 60661
Telephone: (312) 775-8000
Facsimile: (312) 775-8100

CLAIMS APPENDIX

1. A method of verifying a state of an element comprising:

determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element; and

outputting a valid signal if the state of the element is equal to said expected state, wherein the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick.

2. (Cancelled).

3. (Cancelled).

4. The method of claim 1, including sensing the state of the element.

5. The method of claim 1, including generating a high signal if the state of the element is equal to said expected state.

6. The method of claim 1, including generating a low signal if the state of the element is not equal to said expected state.

7. The method of claim 1, wherein determining the state of the element includes determining states of first and second thin oxide gated fuses.

8. The method of claim 1, wherein outputting a valid signal includes determining if the states of both first and second thin oxide gated fuses is equal to a first and second expected states.

9. A method for verifying a state of a memory device comprising:

comparing a state of a first thin oxide gated fuse having an oxide that is less than 2.5 nm thick to a first expected state, and generating a first signal, wherein the state is a state of electrical resistance;

comparing a state of a second thin oxide gated fuse having an oxide that is less than 2.5nm thick to a second expected state, and generating a second signal, wherein the state is a state of electrical resistance; and

outputting a valid signal if both said first and second signals are the same.

10. The method of Claim 9, including outputting a valid signal if both said first and second signals are high.

11. (Cancelled)

12. (Cancelled)

13. The method of Claim 9, including determining if said state of said first thin oxide gated fuse is equal to said first expected state.

14. (Original) The method of Claim 9, including determining if said state of said second thin oxide gated fuse is equal to said second expected state.

15. The method of Claim 9, including mirroring reference and fuse currents.

16. The method of Claim 15, including comparing said reference and fuse currents.

17. A method for verifying a state of a thin oxide gated fuse memory device, comprising:

setting a first expected state;

sensing a state of a first thin oxide gated fuse having an oxide that is less than 2.5nm thick, wherein the state is a state of electrical resistance;

determining if said state of said first thin oxide gated fuse is equal to said first expected state and generating a first signal;

setting a second expected state;

sensing a state of a second thin oxide gated fuse having an oxide that is less than 2.5nm thick, wherein the state is a state of electrical resistance;

determining if said state of said second thin oxide gated fuse is equal to said second expected state and generating a second signal; and

generating a valid output if both said first and second signals are the same.

18. (Cancelled)

19. (Cancelled)

20. A memory device comprising:

at least one memory cell having at least one thin oxide gated fuse having an oxide that is less than 2.5nm thick;

at least one reference cell;

at least one verify circuit connected to said memory cell and said reference cell sensing a state of said at least one thin oxide gated fuse, wherein the state is a state of electrical resistance;

at least one exclusive nor gate connected to said verify circuit; and

a logic gate connected to said exclusive nor gate generating a valid signal.

21. The method of claim 1, wherein the verify circuit comprises a current amplifier.

22. The method of claim 1, wherein the thin oxide gated fuse having an oxide that is less than 2 nm thick.

EVIDENCE APPENDIX

There are no pages in this appendix

RELATED PROCEEDINGS APPENDIX

There are no pages in this Appendix.